at least one semiconductor chip having a first main surface and a second main surface opposite and parallel to the first main surface, said first and second main surfaces being sandwiched between and in parallel with a predetermined two power terminals of said at least three power terminals, such that the first and second main surfaces of the at least one semiconductor chip are electrically connected to the predetermined two power terminals without bonding wires.

11. (Twice Amended) A semiconductor device comprising:

at least three power terminals provided one above another; and

at least one semiconductor chip having a first main surface and a second main surface opposite and parallel to the first main surface, said first and second main surfaces being sandwiched between and in parallel with a predetermined two power terminals of said at least three power terminals, such that the first and second main surfaces of the at least one semiconductor chip are electrically connected to the two power terminals without bonding wires,

wherein the first main surface of said at least one semiconductor chip interposed between said two power terminals is connected to one power terminal of said two power terminals by soldering or pressure welding, and the second main surface is connected to another power terminal of said two power terminals by soldering or pressure welding.

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-19 are pending in the present application with Claims 1 and 11 having been amended by the present amendment.